WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a plurality of terminals including an output terminal and at least one input terminal; and

a configurable voltage regulator operable in a first mode or a second mode, comprising:

output driver circuitry, having an output coupled to the output terminal;

a first regulator mode control circuit, having at least one input coupled to an input terminal, having an output coupled to the output driver circuitry;

a second regulator mode control circuit, having at least one input coupled to an input terminal, and having an output coupled to the output driver circuitry; and

configuration circuitry, for selectably enabling the first and second regulator mode control circuits responsive to a configuration signal.

2. The integrated circuit of claim 1, wherein the configuration circuitry comprises:

a writable configuration register, coupled to the at least one configuration switch, for receiving and storing configuration data indicating the selected mode.

3. The integrated circuit of claim 1, wherein the first regulator mode control circuit comprises switching regulator control circuitry, comprising:

an error amplifier having a first input coupled to a first input terminal, having a second input receiving a reference voltage, and having an output;

a first comparator receiving the output of the error amplifier at one input, and receiving a reference voltage at another input, and having an output coupled to the

output driver, for providing an output signal responsive to a comparison of the error amplifier output to the reference voltage.

4. The integrated circuit of claim 3, wherein the reference voltage is a triangle waveform.

5. The integrated circuit of claim 4, wherein the switching regulator control circuitry further comprises:

a second comparator, receiving the reference voltage at one input and a control voltage at another input;

logic circuitry, having inputs coupled to the output of the first and second comparators, for generating an output driver control signal to the output driver responsive to the outputs of the first and second comparators.

6. The integrated circuit of claim 3, further comprising:

a fault amplifier, having an input coupled to the output of the error amplifier, for generating a fault signal responsive to the signal at the error amplifier output.

7. The integrated circuit of claim 3, wherein the output driver circuitry comprises:

first and second transistors having conduction paths connected in series, and having the output terminal connected to a node between their conduction paths, and having control terminals coupled to the output of the first comparator.

8. The integrated circuit of claim 9, further comprising:

output drive control circuitry, coupled to the output of the first comparator and to the control terminals of the first and second transistors, for controlling the first and second transistors in a complementary fashion.

9. The integrated circuit of claim 3, further comprising:

third and fourth transistors, having conduction paths connected in series and to a second output terminal, and having control terminals; and

wherein the configuration circuitry further comprises:

first and second configuration switches, for applying a disabling voltage to the control terminals of the third and fourth transistors when the switching regulator control circuitry is enabled.

10. The integrated circuit of claim 1, wherein the second regulator mode control circuit comprises charge pump regulator control circuitry, comprising:

an error amplifier, having a first input coupled to an input terminal, and having a second input receiving a reference voltage, and having an output; and

pulse width modulation circuitry, having an input coupled to the output of the error amplifier, and having an output coupled to the output driver circuitry, for controlling the output driver circuitry responsive to the output of the error amplifier.

11. The integrated circuit of claim 10, wherein the charge pump regulator control circuitry further comprises:

a voltage divider, coupled to the input terminal, for applying a first sense voltage to the first input of the error amplifier responsive to the voltage at the input terminal.

12. The integrated circuit of claim 11, wherein the voltage divider provides a plurality of taps;

wherein the first input of the error amplifier is coupled to a first tap of the voltage divider;

wherein the charge pump regulator control circuitry further comprises:

a fault comparator, having a first input coupled to a second tap of the voltage divider and a second input coupled to the reference voltage, for generating a

fault signal responsive to a comparison of the voltage at the second tap of the voltage divider and the reference voltage.

13. The integrated circuit of claim 12, the charge pump regulator control circuitry further comprises:

configuration switches, for coupling selected ones of the taps of the voltage dividers to the fault comparator and error amplifier responsive to the configuration circuitry.

14. The integrated circuit of claim 10, further comprising:

third and fourth transistors, having conduction paths connected in series and to a second output terminal, and having control terminals; and

wherein the configuration circuitry further comprises:

first and second configuration switches, for coupling the control terminals of the third and fourth transistors to the pulse width modulation circuitry responsive to the charge pump regulator control circuitry is enabled.

15. A method of generating a regulated voltage, comprising the steps of:

configuring a configurable voltage regulator in an integrated circuit into either a switching regulator mode or a charge pump regulator mode, the configurable voltage regulator comprising output drive circuitry having outputs at first and second drive terminals, the output drive circuitry including first and second transistors coupled to the first drive terminal;

in the switching regulator mode:

connecting a drive transistor to the first drive terminal;

connecting an external network including an inductor to the transistor, the external network producing the regulated voltage;

connecting an error amplifier of the voltage regulator to the external network, so that the error amplifier receives a voltage corresponding to the regulated voltage; and

disabling third and fourth transistors coupled to the second drive terminal;

in the charge pump regulator mode:

connecting a flyback capacitor to the first and second drive terminals;

enabling third and fourth transistors coupled to the second drive terminal, the fourth transistor coupled between the second drive terminal and a sense terminal;

connecting a load at the sense terminal;

coupling an error amplifier of the voltage regulator to the sense terminal, so that the error amplifier receives a voltage corresponding to the regulated voltage;

responsive to the configuring step configuring the configurable voltage regulator in the switching regulator mode:

coupling the output of the error amplifier to switching regulator control circuitry; and

coupling the output of the switching regulator control circuitry to the output drive circuitry so that the first and second transistors are driven by the switching regulator control circuitry responsive to the error amplifier; and

responsive to the configuring step configuring the configurable voltage regulator in the charge pump regulator mode:

coupling the output of the error amplifier to pulse width modulation circuitry; and

operating the pulse width modulation circuitry responsive to the error amplifier output to drive the first, second, third, and fourth transistors.

16. The method of claim 15, wherein the configuring step comprises:

writing configuration information to a configuration register.

17. The method of claim 15, further comprising, in the switching regulator mode:

comparing an output of the error amplifier to a time-varying waveform in the switching regulator control circuitry to generate a time-varying signal corresponding to the comparing; and

coupling the time-varying signal to the first and second transistors.

18. The method of claim 17, further comprising, in the switching regulator mode:

generating a maximum duty cycle signal; and

gating the coupling of the time-varying signal to the first and second transistors with the maximum duty cycle signal.

19. The method of claim 17, further comprising, in the switching regulator mode:

generating a fault signal responsive to the output of the error amplifier exceeding a fault level.

20. The method of claim 15, further comprising, in the charge pump regulator mode:

coupling the sense terminal to a voltage divider having a plurality of taps, wherein a first one of the taps is coupled to the error amplifier; and

generating a fault signal responsive to a voltage at a second one of the taps exceeding a fault level.

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